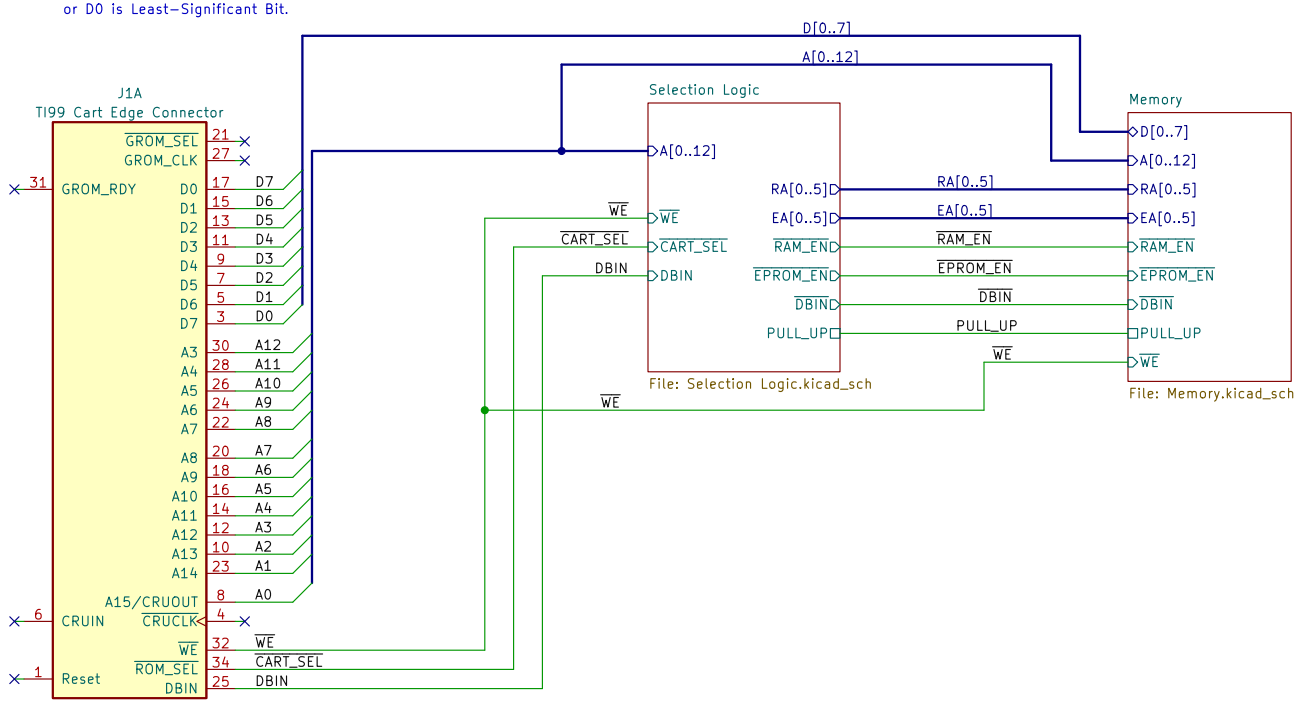
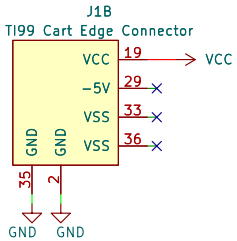
NOTE:

Connector Address and Data Pins Use
Texas Instruments Convention Where
A0 or D0 is Most-Significant Bit.

Schematic Address and Data Buses
Use Intel Convention Where A0
or D0 is Least-Significant Bit.



Power Connections

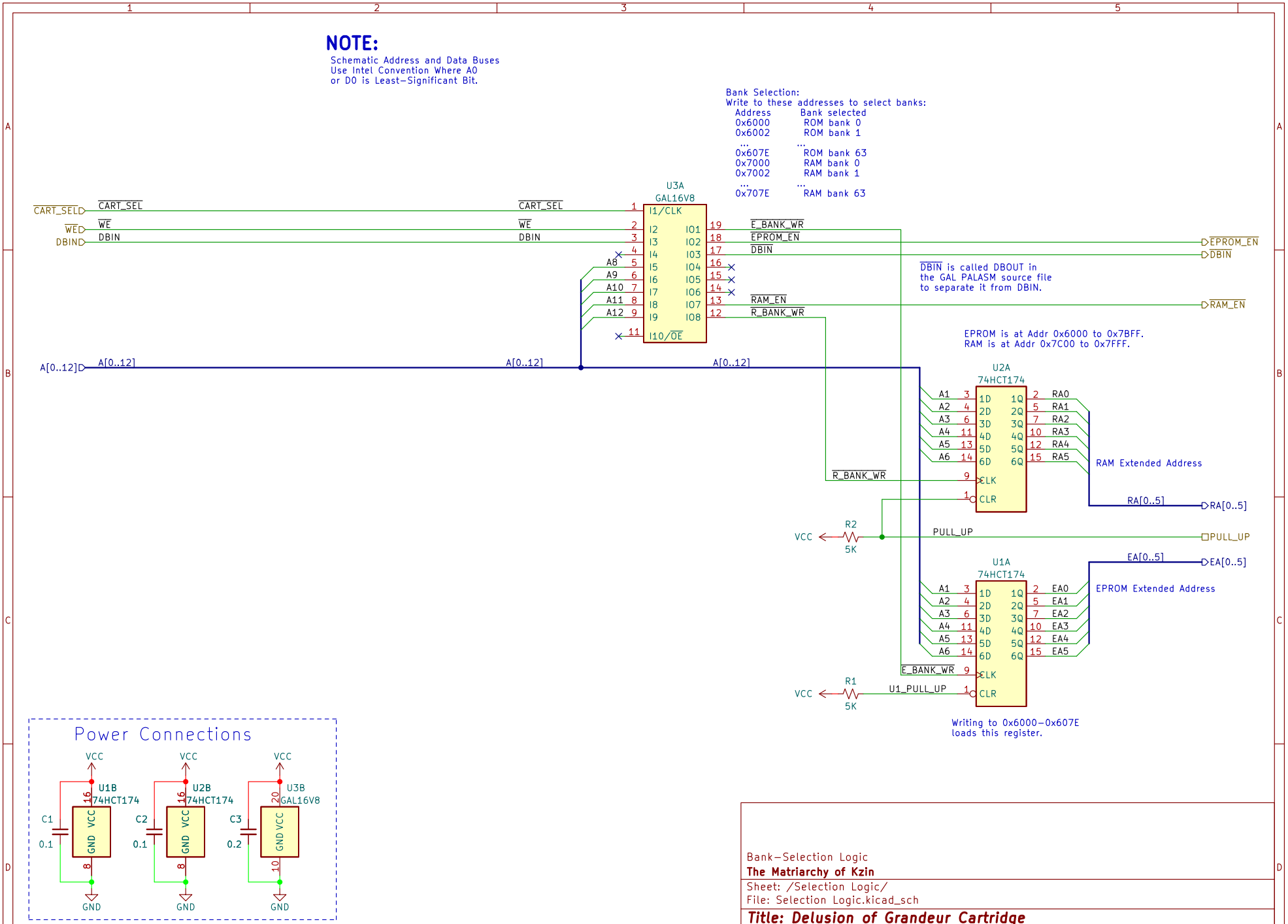


Unused Gates (None)

Overview
The Matriarchy of Kzin
Sheet: /
File: RAM-ROM-PLD Cartridge.kicad_sch

Title: Delusion of Grandeur Cartridge

Size: USLetter	Date: 2024 Feb 27	**Rev: 0**
KiCad E.D.A. kicad 6.0.8+dfsg-1~bpo11+1+rpt1		Id: 1/3



Bank-Selection Logic

The Matriarchy of Kzin

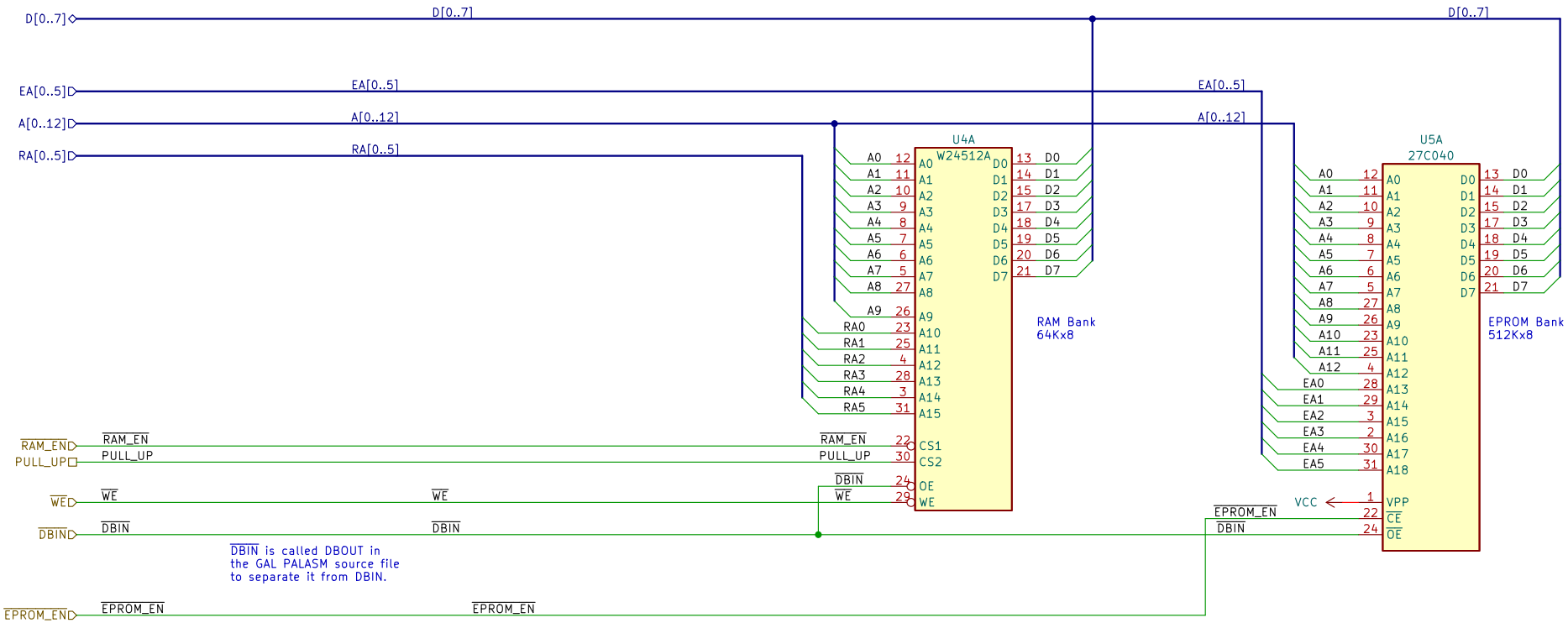
Sheet: /Selection Logic/

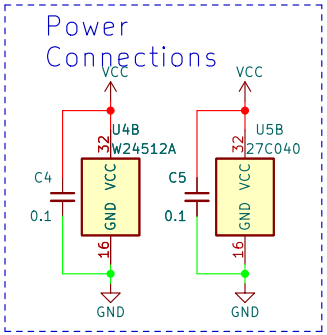
File: Selection Logic.kicad_sch

Title: Delusion of Grandeur Cartridge

Size: USLetter	Date: 2024 Feb 27	**Rev: 0**
KiCad E.D.A. kicad 6.0.8+dfsg-1~bpo11+1+rpt1		Id: 2/3

NOTE:
Schematic Address and Data Buses
Use Intel Convention Where A0
or D0 is Least-Significant Bit.





Memory
The Matriarchy of Kzin
Sheet: /Memory/
File: Memory.kicad_sch

Title: Delusion of Grandeur Cartridge

Size: USLetter	Date: 2024 Feb 27	**Rev: 0**
KiCad E.D.A. kicad 6.0.8+dfsg-1~bpo11+1+rpt1		Id: 3/3