NOTES: UNLESS OTHERWISE SPECIFIED:

1. SEE SHEET 2 FOR SEQUENTIAL LOGIC.
   SEE SHEET 3 FOR COMBINATIONAL LOGIC.
2. THESE DRAWINGS DESCRIBE THE LOGIC OF THE HOMBRE I.C. SPECIFIED IN T.I. PART NO. 1049723.
3. THE PIN ASSIGNMENTS ARE AS FOLLOWS:

PIN #	I/O	BUFFER	PIN NAME	FUNCTION
1	O	BF2A	VCSR*	ACTIVE LO VDP CHIP READ CS
2	O	BF2A	VCSW*	ACTIVE LO VDP CHIP WRITE CS
3	I	BF1A	A0	CPU ADDRESS BUS LINE(MOST SIGNIFICANT BIT)
4	I	BF1A	A1	CPU ADDRESS BUS LINE
5	I	BF1A	A2	CPU ADDRESS BUS LINE
6	I	BF1A	A3	CPU ADDRESS BUS LINE
7	I	BF1A	A4	CPU ADDRESS BUS LINE
8	I	BF1A	A5	CPU ADDRESS BUS LINE
9	O	BF2A	ROMG*	ACTIVE LO DECODE FOR COMMAND MODULE ROM MEMORY SPACE
10			GND	GROUND
11	O	BF2A	ROMEN*	ACTIVE LO 4K INTERNAL ROM CS
12	O	BF2A	RAMCS*	ACTIVE LO CPU SCRATCHPAD RAM CHIP SELECT
13	O	BF2A	NNOICS*	ACTIVE LO TMS9901 CHIP SELECT
14	I	BF1A	DBIN	CPU DATA BUS DIRECTION CONTROL SIGNAL. HI=DATA TO CPU, LO=DATA FROM CPU
15	I	BF1A	MEMEN*	CPU MEMORY ENABLE CONTROL SIGNAL (ACTIVE LO)
16	I	BF1A	CWE*	CPU MEMORY WRITE ENABLE (ACTIVE LO)
17	O	BF2A	MBE*	ACTIVE LO MEMORY BLOCK ENABLE FOR I/O PORT PERIPHERAL PAGED MEMORY SYSTEM
18	O	BF2A	GCS*	ACTIVE LO GROM CHIP SELECT CS
19	O	BF2A	GBEN*	ACTIVE LO COMMAND MODULE/GROM DATA BUS DRIVER ENABLE
20	O	BF2A	SNDCS*	ACTIVE LO SOUND CHIP SELECT
21	O	BF2A	VCC	POWER +5V
22	O	BF2A	SBE	ACTIVE HI SPEECH BLOCK ENABLE TO I/O PORT
23	O	BF2A	URST*	UNSYNCHRONIZED RESET (ACTIVE LO)
24	I	BF1A	GRY	GROM CHIP READY OUTPUT. NORMALLY LO, ACTIVE HI
25	I	BF1A	PHI2*	3MHz CLOCK PHASE #2, ACTIVE LO, 25% DUTY
26	I	BF1A	PHI4*	3MHz CLOCK PHASE #4, ACTIVE LO, 25% DUTY
27	O	BF2A	CPURY	READY SIGNAL TO CPU
28	I	BF1A	CMIN*	COMMAND MODULE PLUGGED IN SIGNAL, LO INDICATES A C/M IS PLUGGED IN
29	I	BF1A	INIT*	TEST PIN USED TO INITIALIZE ALL FLIP FLOPS ACTIVE LO, IS TIED HI IN THE 99/4 SYSTEM
30	I	BF1A	SYSRY	SYSTEM READY, HI IS READY MODE
31			GND	POWER GROUND
32	O	BF2A	A15/CRUOUT	MULTIPLEXED A15 AND CRUOUT. IF MEMEN* IS ACTIVE, A15 IS GATED THROUGH
33	I	BF1A	CRUOUT	CPU CRU DATA OUTPUT LINE
34	I	BF1A	PUP	POWER IS UP ACTIVE HI. CONNECTS TO A SERIES RC NETWORK MID-POINT
35	O	BF2A	LSVREN*	LEAST SIGNIFICANT SAVE REGISTER ENABLE (ACTIVE LO)
36	O	BF2A	LWEN*	LEAST SIGNIFICANT DATA BYTE WRITE ENABLE (ACTIVE LO)
37	O	BF2A	MBYEN*	MOST SIGNIFICANT DATA BYTE ENABLE (ACTIVE LO)
38	O	BF2A	WE*	SYSTEM WRITE ENABLE (ACTIVE LO)
39	I	BF1A	PHI1*	3MHz CLOCK PHASE #1, ACTIVE LO, 25% DUTY
40			VCC	POWER +5V

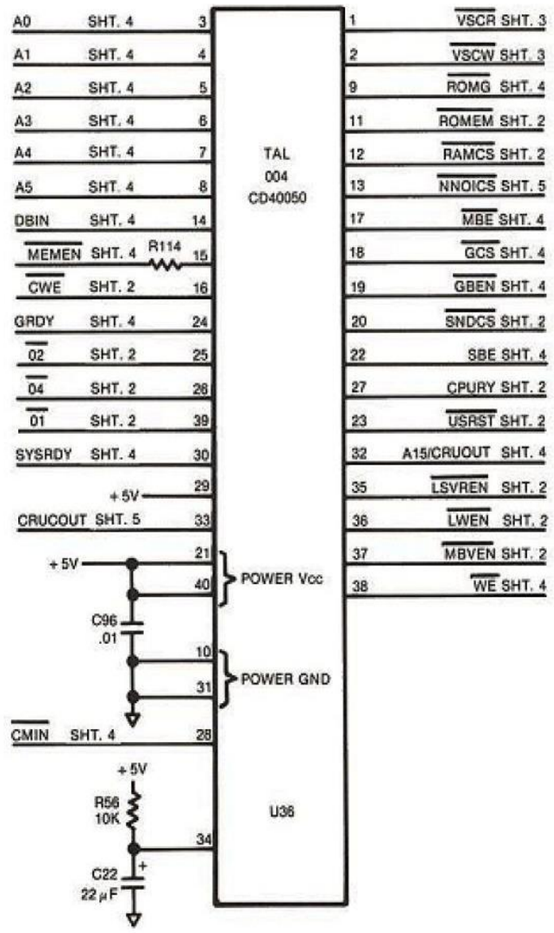

FIGURE J. TI-99/4QI SCHEMATIC DIAGRAM

Designates signal name connection between sequential/combinatorial logic sheets. Small text is XY location-Page.

Designates input/output of physical TAL package pin#.

Designates TAL logic (NOT function NAND-based logic).

Designates TAL output buffer driver and boolean equivalent NOT. For timing, additional gates added in signal path.

Boolean intermediate/cumulative logic for clarity. CWE + DBIN

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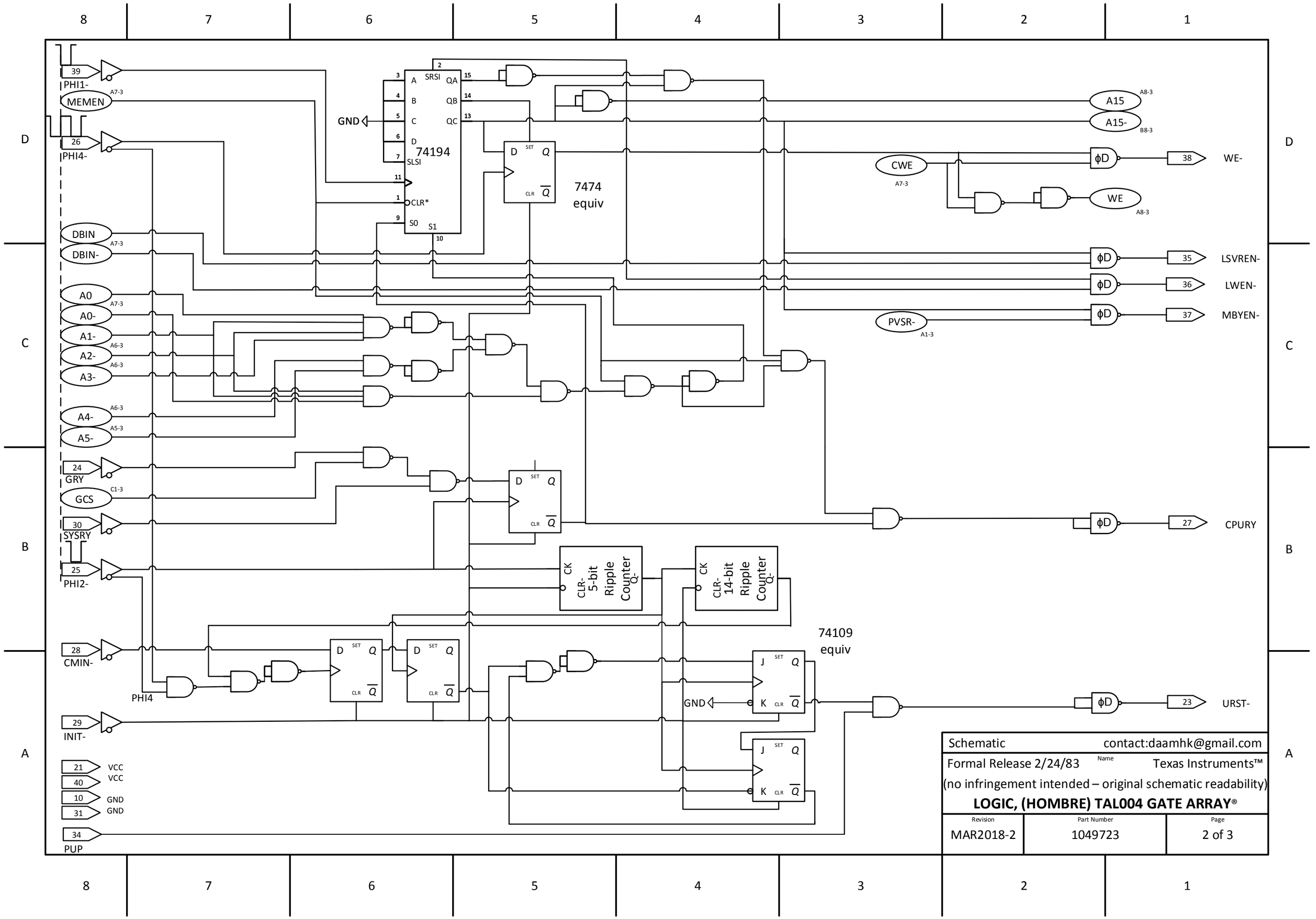
8
7
6
5
4
3
2
1
D
C
B
A
39
PHI1-
MEMEN
A7-3
26
PHI4-
GND
2
3
4
5
6
7
11
1
9
10
15
14
13
A
SRSI
B
C
D
SLSI
CLR*
S0
S1
QA
QB
QC
74194
D
SET
Q
CLR
7474
equiv
A15
A8-3
A15-
B8-3
CWE
A7-3
ϕD
38
WE-
WE
A8-3
DBIN
DBIN-
A0
A0-
A1-
A6-3
A2-
A3-
A4-
A5-
A5-3
35
LSVREN-
36
LWEN-
PVSR-
A1-3
37
MBYEN-
24
GRY
C1-3
GCS
30
SYSRY
27
CPURY
25
PHI2-
CK
CLR-
5-bit
Ripple
Counter
Q-
14-bit
28
CMIN-
PHI4
J
K
74109
equiv
GND
23
URST-
29
INIT-
21
VCC
40
VCC
10
GND
31
GND
34
PUP
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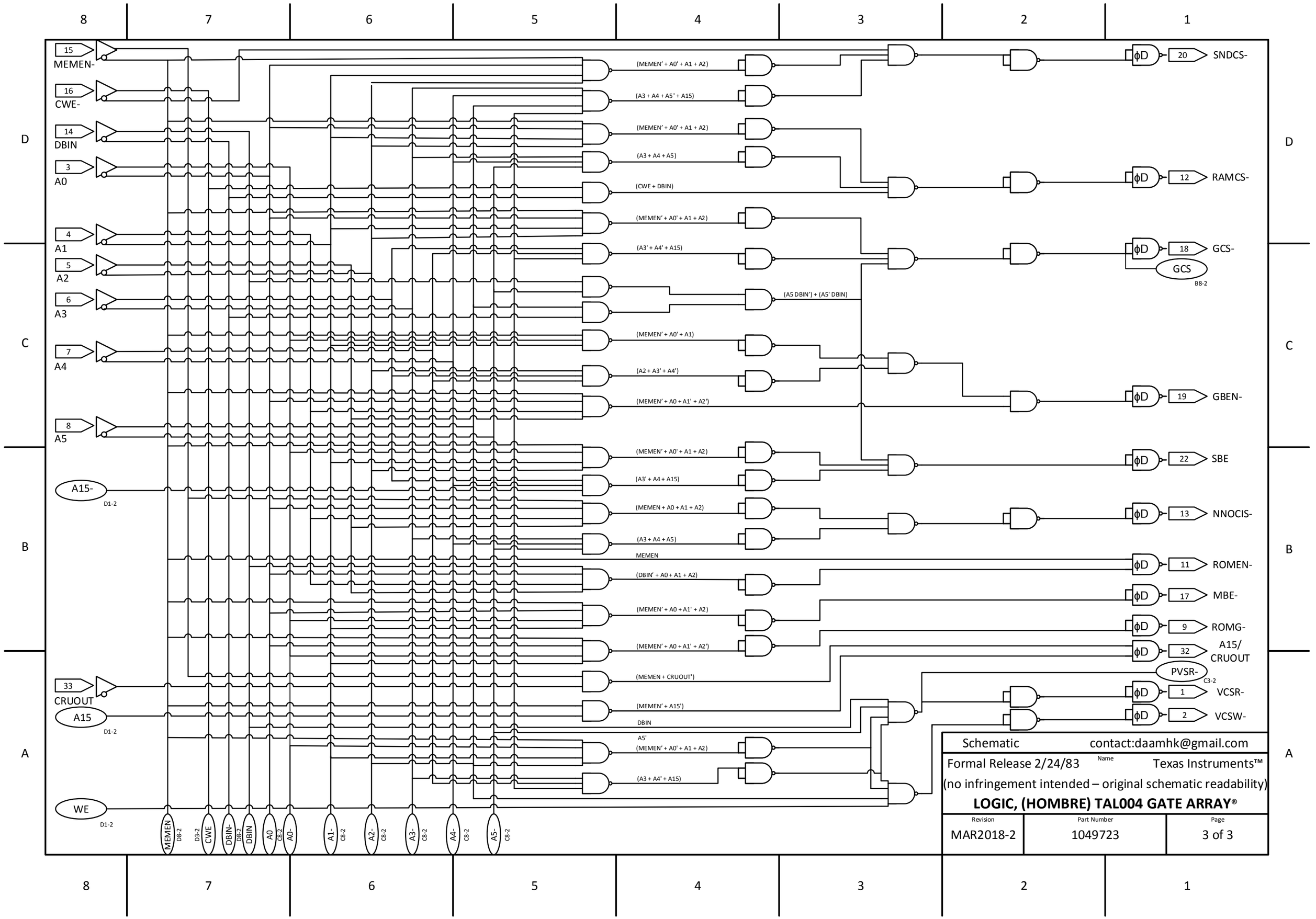
15
MEMEN-
16
CWE-
14
DBIN
3
A0
4
A1
5
A2
6
A3
7
A4
8
A5
A15-
D1-2
33
CRUOUT
A15
D1-2
WE
D1-2
MEMEN D8-2
D3-2
CWE
DBIN- D8-2
DBIN D8-2
A0 C8-2
A0- C8-2
A1- C8-2
A2- C8-2
A3- C8-2
A4- C8-2
A5- C8-2
(MEMEN' + A0' + A1 + A2)
(A3 + A4 + A5' + A15)
(MEMEN' + A0' + A1 + A2)
(A3 + A4 + A5)
(CWE + DBIN)
(MEMEN' + A0' + A1 + A2)
(A3' + A4' + A15)
(A5 DBIN') + (A5' DBIN)
(MEMEN' + A0' + A1)
(A2 + A3' + A4')
(MEMEN' + A0 + A1' + A2')
(MEMEN' + A0' + A1 + A2)
(A3' + A4 + A15)
(MEMEN + A0 + A1 + A2)
(A3 + A4 + A5)
MEMEN
(DBIN' + A0 + A1 + A2)
(MEMEN' + A0 + A1' + A2)
(MEMEN' + A0 + A1' + A2')
(MEMEN + CRUOUT')
(MEMEN' + A15')
DBIN
A5'
(MEMEN' + A0' + A1 + A2)
(A3 + A4' + A15)
ϕD
20
SNDCS-
ϕD
12
RAMCS-
ϕD
18
GCS-
GCS
B8-2
ϕD
19
GBEN-
ϕD
22
SBE
ϕD
13
NNOCIS-
ϕD
11
ROMEN-
ϕD
17
MBE-
ϕD
9
ROMG-
ϕD
32
A15/
CRUOUT
PVSR-
C3-2
ϕD
1
VCSR-
ϕD
2
VCSW-
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